AMENDMENTS TO THE SPECIFICATION

1. Please **replace** the paragraph on page 12, starting on line 14, with the following:

Referring now to Figure 2, in order to generate a positive charge in the body of the NMOS transistor of Figure 1, the gate voltage V_g and drain voltage V_d, as well as the source voltage, are initially zero. At time t_0, the gate voltage is brought to -1.5V and at time $t_0 + \underline{\Delta}t_0$ (where $\underline{\Delta}t_0$ can be greater than, less than or equal to zero), the drain voltage V_d is brought to -2V, while the source voltage remains at zero. By applying a negative voltage pulse to the gate and a more negative voltage pulse to the drain, a concentration of negative charge forms in the body 20 in the vicinity of the gate 28, while a concentration of positive charge forms in the body in the vicinity of insulating layer 12. At the same time, a conduction channel linking the source 18 and drain 22 forms in the body 20, allowing conduction of electrons between the source 18 and drain 22. This allows electrons to be attracted into the channel from the source 18 and/or drain 22.

2. Please **replace** the paragraph on page 13, starting on line 6, with the following:

The drain voltage V_d then returns at time t_1 to zero, and the gate voltage V_g returns to zero at $t_1 + \underline{\Delta}t_1$ to remove the conductive channel between the source 18 and drain 22, the time interval $t_1 - t_0$ typically being between a few nanoseconds and several tens of nanoseconds, while $\underline{\Delta}t_1$ is of the order of 1 nanosecond. It is also possible to create a positive charge in the body 20 by applying a positive drain voltage pulse, depending upon the voltages of the source, drain and gate relative to each other. It has been

found in practice that in order to create a positive charge in the body, the drain voltage must be switched back to zero before the gate voltage.

3. Please replace the paragraph on page 13, starting on line 14, with the following:

Referring now to Figure 3, a negative charge is generated in the body 20 by increasing the gate voltage V_g to +1V at t_0 while the source and drain voltages are held at zero, then reducing the drain voltage V_d to -2V at time $t_0 + \underline{\Delta}t_0$ while the source voltage is held at zero. The gate voltage V_g and drain voltage V_d are then subsequently brought to zero at times t_1 and $t_1 + \underline{\Delta}t_1$ respectively, where $\underline{\Delta}t_1$ can be positive or negative (or zero). The application of a positive voltage to the gate 28 relative to the voltages applied to the source 18 and drain 22 again causes the formation of a conductive channel between the source 18 and drain 22, as was the case with the formation of an excess positive charge as described above with reference to Figure 2. The positive voltage applied to the gate 28 also creates a concentration of negative charge in the body 20 in the vicinity of the gate 28, and a concentration of positive charge in that part of the body remote from the gate 28, i.e., adjacent the insulating layer 12.

4. Please replace the paragraph on page 20, starting on line 22, with the following:

A further possibility is shown in Figure 12, which shows the levels achievable using the charge pumping principle described with reference to Figures 6 and 7. The amount of charge removed after each pulse causes a current decrease of $\underline{\Delta}I_S$, and the various levels can be obtained by changing the number of charge pumping pulses.